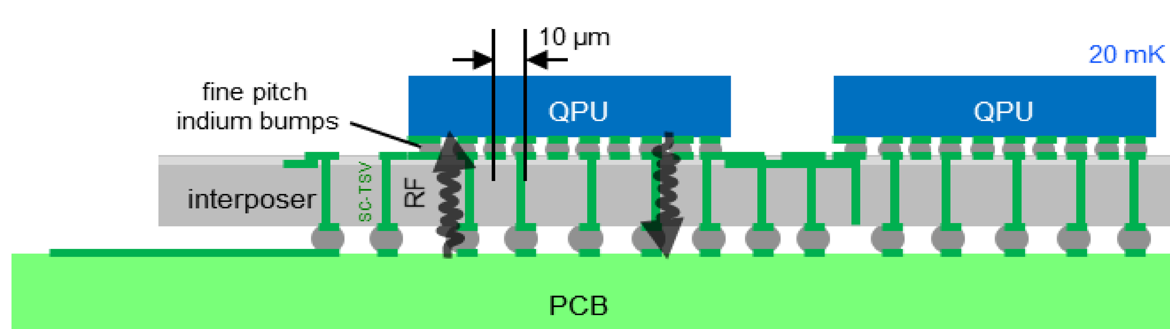
moduleqnc
quantum & neuromorphic computing

Cryogenic routing and interposer technologies

1 Challenges and enabling technologies

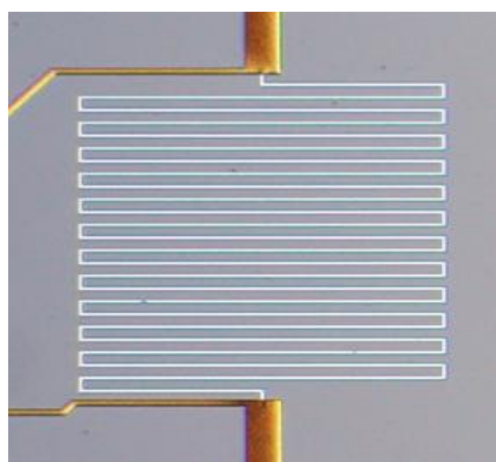
Increasing complexity and number of qubits require scalable integration concepts

Challenges:
- Electromagnetic and thermal shielding, hardware architecture optimization
- High wiring and interconnection density
- Low-loss interposer substrates for integrating qubit chips and control ICs, minimizing signal loss to improve operational fidelity.
- Superconducting multilayer wiring and through-via of interposer substrates.
- Superconducting flip chip interconnects for scalable 3D integration and stacking
- Superconducting flex cables as connection to outside
- High-frequency-compatible cable routing with shielding

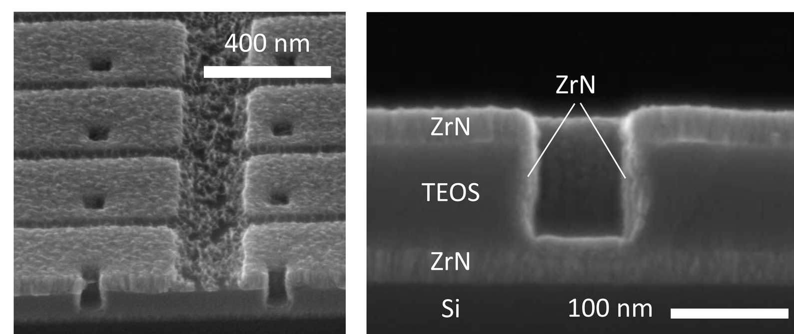


2 Interposer for 3D Integration

Superconducting multilayer wiring and through-vias in interposer substrates are needed for 3D integration and stacking of QPUs and controller. This will require:
- Superconductive metal lines with high critical current density (e.g. Nb, NbN)
- Multilayer thinfilm redistribution layers (e.g. Nb, ZrN)
- Superconductive through vias (e.g. Nb)



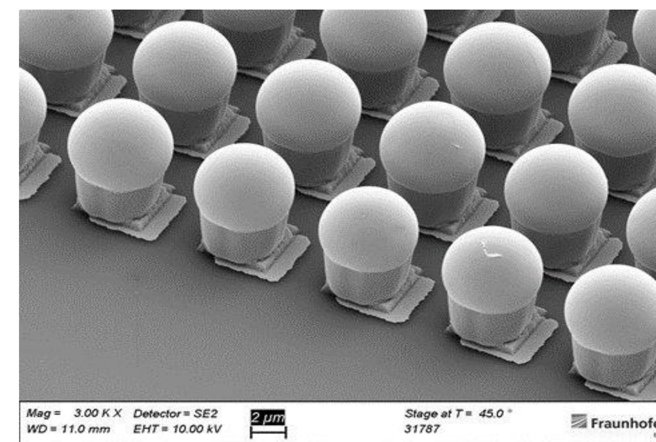
Niobium and niobium/ gold routing



SEM crosssection of two insulated ZrN layers with vertical interconnect for multilevel superconducting wiring

3 Flip Chip Integration

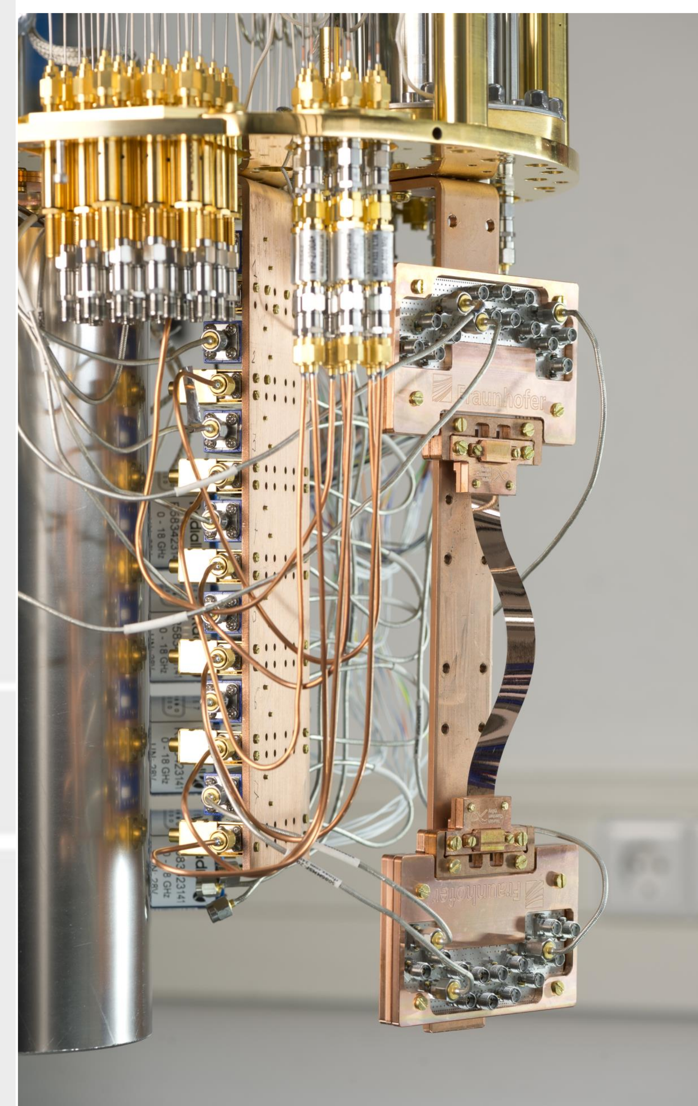
Flip chip interconnects must withstand thermo-mechanically large temperature changes into cryogenic temperature range. It should also provide superconductivity and fine pitch capability.
- Indium and indium/tin bumping best known for cryogenics
- Fine pitch capability down to 10 µm.
- Flip chip bonding temperature down to room temperature and fluxless reflow soldering
- Superconductive below 3.4K (In) and 5.4K (InSn)



Indium 10µm pitch:
- Homogeneous height
- Oxide removal
- Fluxless bonding
- High interconnect yield

4 High Density Wiring

Use of connections based on flexible foils and high-density PCB direct connectors



- Significantly increased line density (> 80 transmission lines per inch)
- Small cross section (100 µm thick)

➢ High potential for miniaturization
➢ Low thermal conductivity

Fabricated by a role-to-role process

➢ simplified and fast cable manufacturing
➢ increased overall uniformity
➢ Arbitrary length

5 Outlook

- Multilayer rewiring completely with superconductors
- Integration of technologies (bumping and rewiring)
- Reduction of line widths and spacing
- Reduction of bump pitch and increase in the number of contacts
- Thermal decoupling between interposer chips

For inquiries, email us at experts@module-qnc.de

SPONSORED BY THE
Federal Ministry of Education and Research