moduleqnc
quantum & neuromorphic computing

Non-cryogenic assembly and interconnection technologies

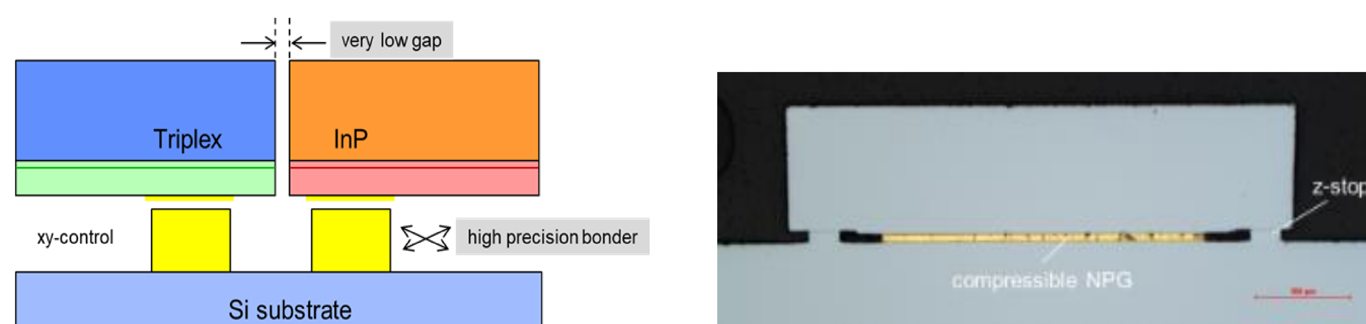
1 Photonic applications

In addition to electrical connections, optoelectronic components (LD, PD) and photonic integrated circuits (PIC) are optically coupled to each other. Passive alignment methods are preferable for scalability of the technology.

Specific integration: optical waveguides, facets, Bragg gratings, deflecting mirrors
- Coupling geometry: e.g. butt coupling, grating coupler, evanescent coupling
- Active and passive alignment methods
- High precision flip chip bonding
- Solder-assisted self-alignment with mechanical stops

2 Passive optical coupling

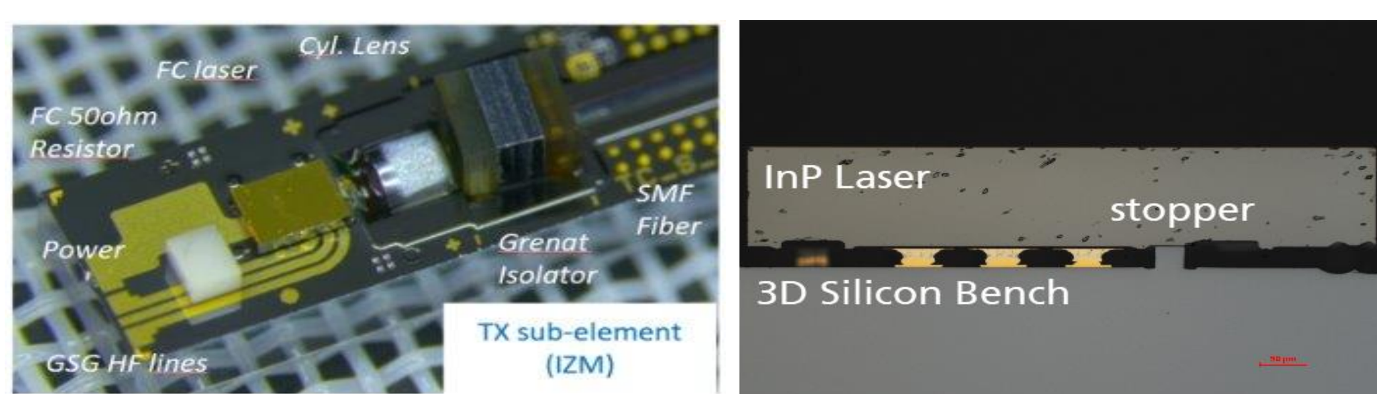
High precision bonding: Chip-to-chip, chip-to-wafer
- Gold-gold thermo-compression with planarized gold bumps
- Nano-porous gold (NPG)
- Lateral bonding accuracy <1µm
- Mechanical stops for height control
- Down to 3µm pitch



Precision bonding with mechanical stops: thermocompression Au-Au or nanoporous gold (NPG)

Thermocompression with nanoporous gold (NPG) and mechanical stops

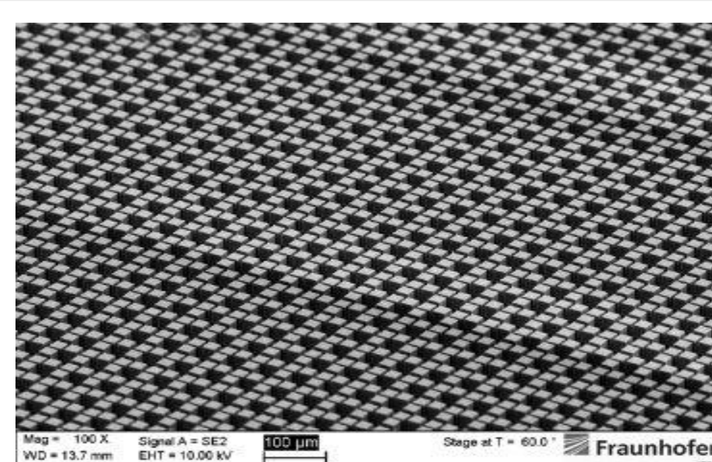
Solder-assisted self-alignment
- AuSn bumping and flip chip up to 20µm pitch
- Design and integration of mechanical stops for self-alignment
- Si, glass, InP, GaN, SiC, GaAs and other wafers



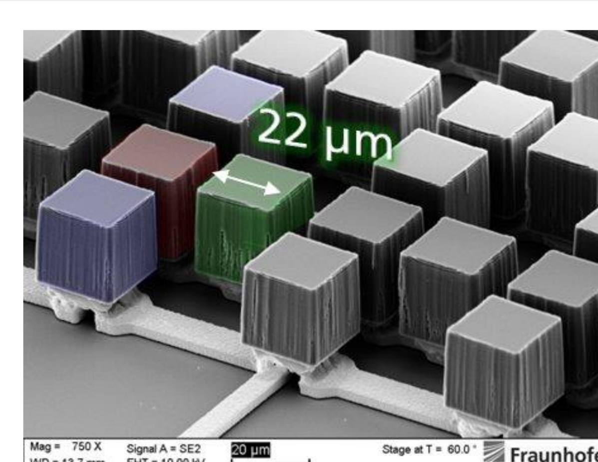
AuSn solder-assisted self-alignment with mechanical stops

3 Micro transfer bonding

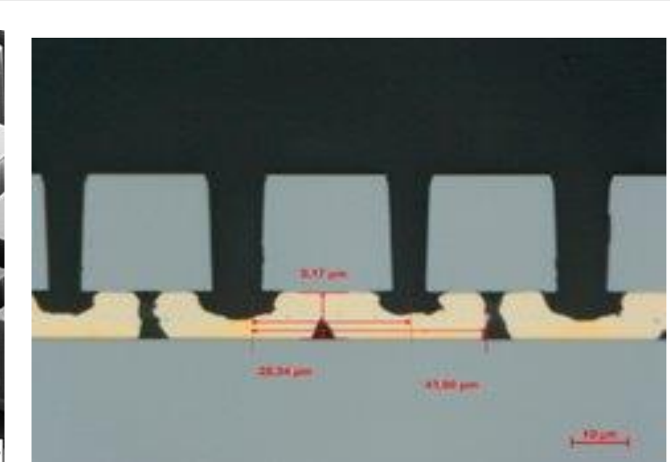
Micro transfer bonding
- Massive parallel assembly
- for small components (up to 20µm)
- with conveyer & laser release
- with AuSn solder or nanoporous gold
- several 1000 components per assembly step



Micro transfer bonding of small chiplets onto a substate



3 different components bonded in 3 steps



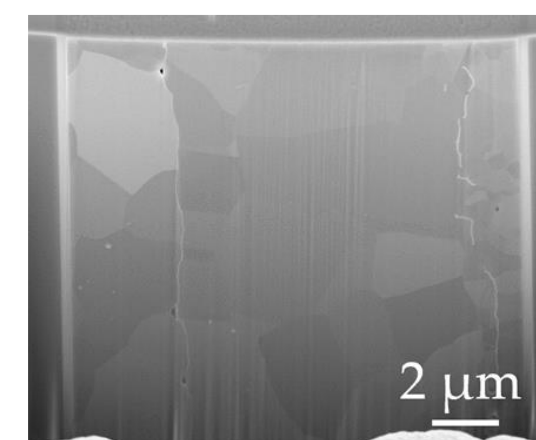
2 AuSn flip chip interconnects per chiplet

4 Wafer to Wafer bonding

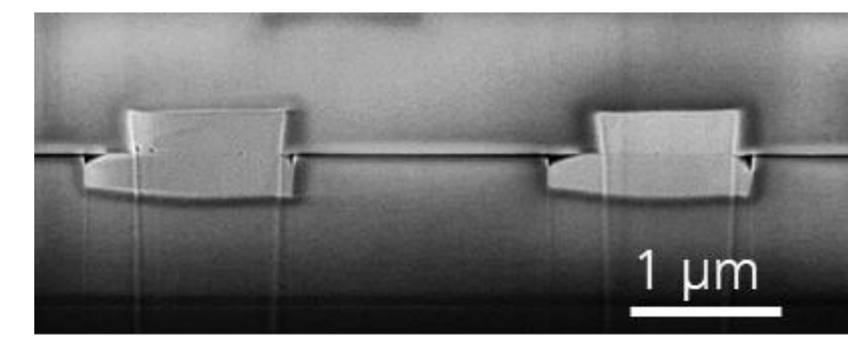
Wafer scale manufacturing of 2.5D/3D highly integrated components e.g. ion traps with integrated optics for laser distribution or traps with multiple layers of electrodes becomes possible. Active electronics can be integrated into ion traps.

Different wafer bonding methods are available:
- Metal bonding, e.g. SLID (Cu-Sn), eutectic (AuSn, AlGe, AuSi), thermocompression (Cu, Au, Al)
- Anodic bonding, e.g. Si-Glass
- Fusion bonding , e.g. Si-Si, Si-LiNbO3/LiTaO3
- Hybrid bonding for high I/O count

They can be applied in combination with TSVs and redistribution layers. Careful pre-treatment is often necessary for a reasonable yield.



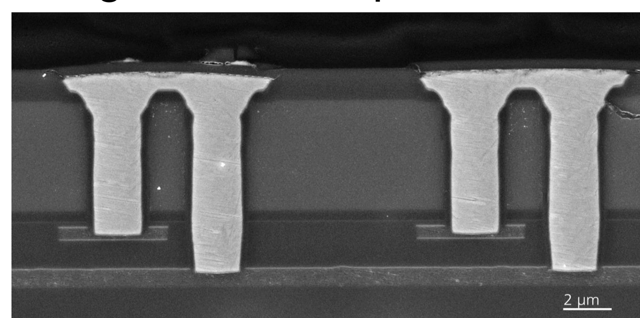
FIB cross section of Al-Al thermocompression bond with electroplated Al-layers can be used for hermetic and electrical integration of different substrate materials



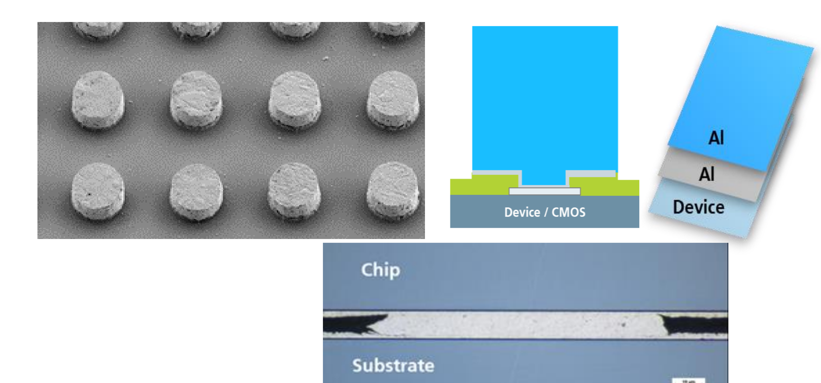
FIB cross section of Cu-SiO2 hybrid bonding for high I/O count applications, e.g. connection of active electronic wafer with electrode wafer of ion traps

5 Flip Chip bonding and Interconnects

Flip Chip bonding and Through Substrate Vias (TSVs) are mandatory for higher integration schemes to realize 3D interconnections. Next to state-of-the-art flip chip bonding technologies, Al ultrasonic bonding is a new promising method which can be performed close to room temperature and without the need of an under bump metallization (UBM).
TSV technology for different aspect ratios will enable the downscaling and electrical integration of various quantum technologies, e.g. integrated ion traps.



µVias filled with Cu to interconnect different layers or even whole wafers



Al pillars for ultrasonic flip chip bonding at room temperature for integration of ASICs without additional UBM

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