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Enabling hybrid AI acceleration: HyDRA

Seamlessly Integrating the Power of Analog Computing in Hybrid (digital/analog) AI Accelerators

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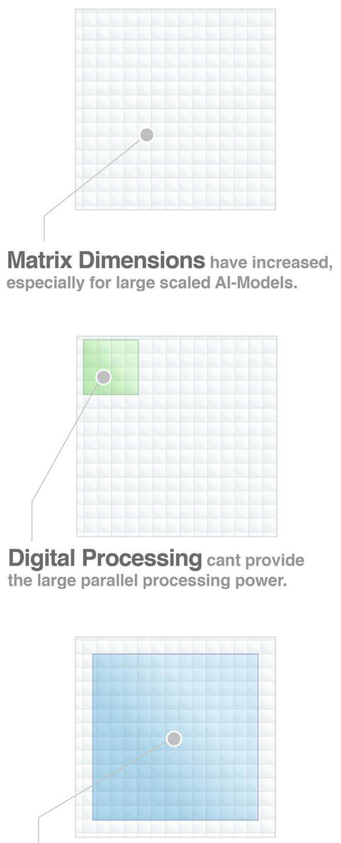
1 Hybrid (D/A/D) AI Accelerators

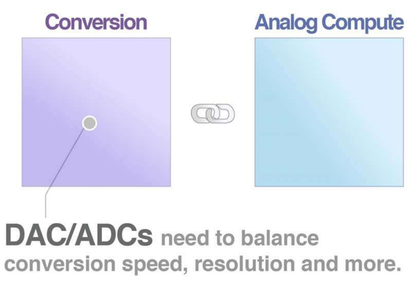
The need of analog matrix computational power

- Neuromorphic hardware aims to emulate AI at hardware level.
- Digital AI-Acceleration is energy inefficient at scale.
- Analog implementations promise energy efficient parallel computations.

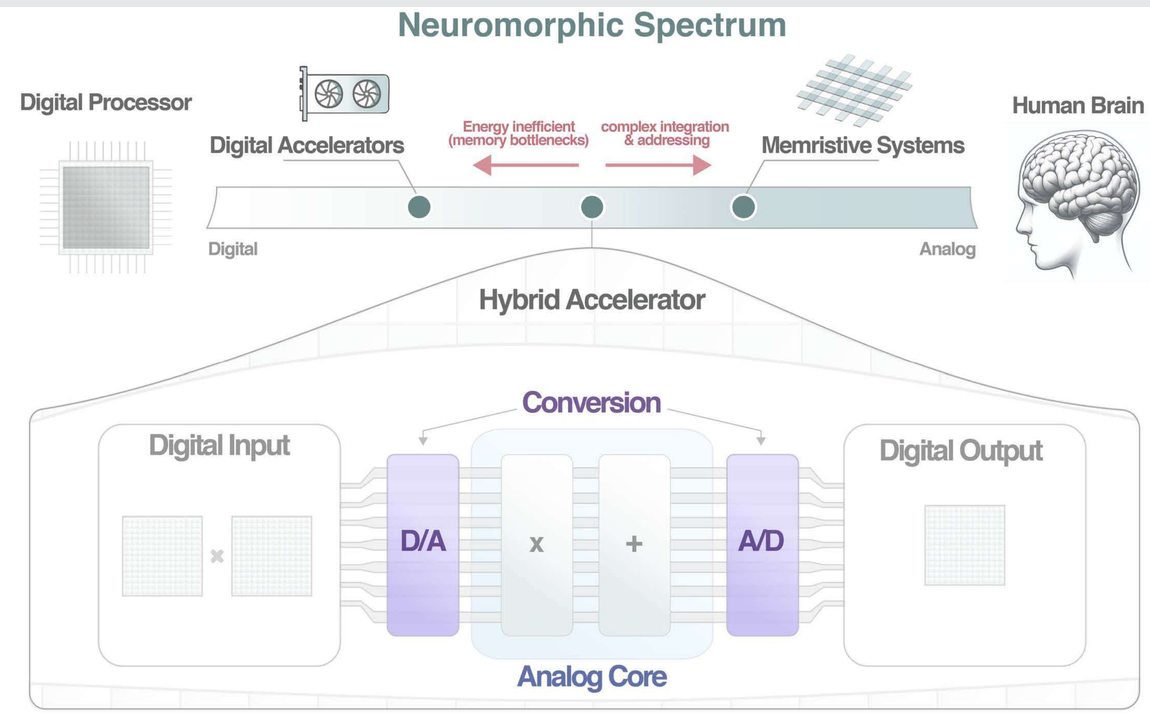


Challenge for analog neuromorphic hardware

- The digital landscape demands conversion from the analog to the digital domain.
- Efficient conversion is key to seamlessly integrate analog hardware without performance loss.



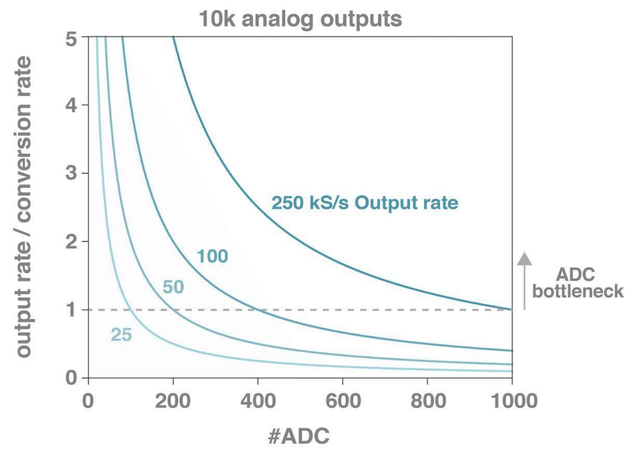
2 Innovation



The hybrid position allows to harness both the benefits of the analog domain and the digital domain, but the conversion bottleneck needs to be addressed.

Why optimized conversion is key

- Analog accelerators require many analog outputs.
- The large number of outputs strain the available conversion rate.
- Area- and energy efficient conversion (e.g. ADC arrays) is key to avoid bottlenecks.

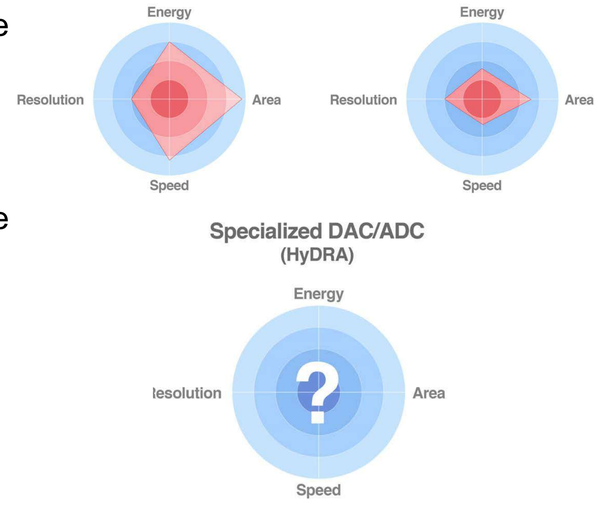


3 Future performance profile & skills of the project partners

Fraunhofer IPMS
Increasing the portfolio of design layouts and expertise in DAC solutions for AI accelerators and analog systems in general (e.g. photonics).

Fraunhofer EMFT & IIS
Increasing the portfolio of design layouts and expertise in ADC solutions for AI accelerators and neuromorphics.

TileCore
Enabling hybrid AI accelerator solutions by combining conversion with in-house developed parallel analog cores.



4 Prospects

Road to scaled hybrid acceleration

- Optimized chip design for conversion solutions as building block.
- Combining these with analog core designs to design hybrid AI accelerators
- Industrially standardized foundry production of hybrid accelerators.
- Enabling energy efficient AI acceleration products.

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